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A Depletion-Load, p-Channel, Bipolar-IGFET Technology

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A high-performance, depletion-load, bipolar-IGFET technology is described. The optimization of device and circuit parameters, the ion-implanted depletion-load fabrication process, and the high-speed input and output circuits, which allow direct interface with the TTL circuit family, are discussed.

I. INTRODUCTION

Since the development of the low-threshold ($V_T = -1$ volt) metal-gate p-channel Al_2O_3-SiO_2 IGFET technology,[1] further technological advances have heen made to improve circuit speed and interface flexihility of IGFET circuits. Two significant improvements have been the incorporation of hipolar-IGFET (BIGFET)[2] devices on the same monolithic silicon-integrated circuit (SIC) and the application of ion implantation to fabricate depletion-load IGFET's.[3] These have resulted in an IGFET technology whose circuits are completely compatihle with the standard 5-volt hipolar TTL family in terms of input and output levels as well as power supply. Furthermore, the relatively high functional packing density of the IGFET technology makes it an extremely attractive option in MSI/LSI applications. These have been successfully realized in the design and fahrication of several Bell System catalog and custom circuits.

In this paper, the technology characteristics of the depletion-load BIGFET technology are deschihed.

II. DEPLETION-LOAD INVERTER

2.1 Circuit characteristics

The advantages of the depletion-load inverter over a similar all-enhancement or resistor-load inverter hecome ohvious when we consider the various load-line characteristics. In Fig. 1, the load lines of a resistive load, an enhancement-IGFET load, and a depletion-IGFET load are shown over the family of IV curves for the enhancement-

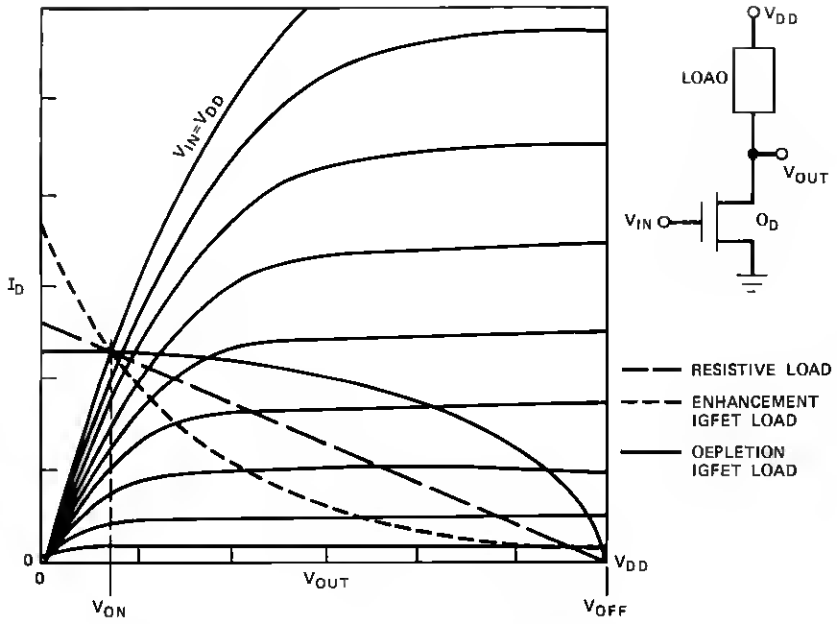

Fig. 1—Inverter load-line characteristics.

IGFET driver (Q_D). The three load lines are chosen to intercept at the same point in the $V_{in} = V_{DD}$ and $V_{in} = 0$ characteristics curves to reflect the fact that they will produce the same output dc levels. The area under the load line represents the transient power dissipated during one logic transition. For a given capacitive loading on the inverter output node, the transient power dissipation is proportional to the frequency of operation. Therefore, the area under the load line is directly proportional to the maximum operating frequency of the inverter. The speed advantage of the depletion load is apparent because it has the largest area between $V_{out} = V_{oo}$ and $V_{out} = V_{off}$.

2.2 *Circuit equations*

In this section, the approximate circuit equations of the depletion-load inverter are reviewed. In spite of their inexactness, they are useful because they provide insight into the functional dependence of circuit parameters on device parameters. However, the final choice of device parameters, discussed in Section 2.3, was based on more exact computer calculations.

Assuming the gradual-channel approximation, the output levels (V_{on} and V_{off}) and the corresponding single-stage noise margins (V_{M1} and V_{M2}) of a depletion-load inverter with Q_D on and off, respectively,

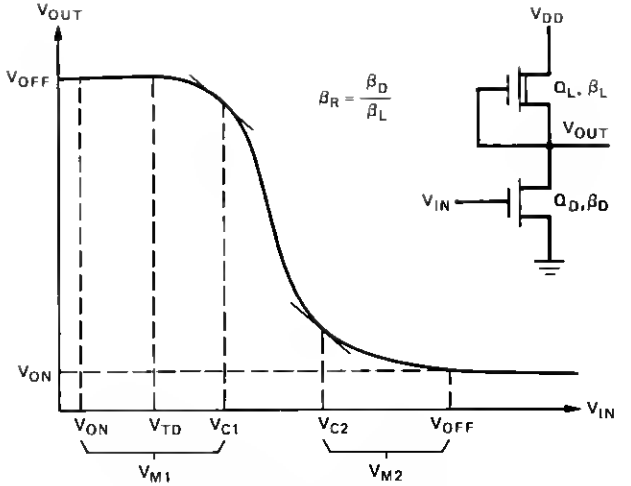

Fig. 2—Depletion load inverter.

as shown in Fig. 2, may be given by[4]

$$V_{on} \cong \frac{V_a^2}{2(V_{DD} - V_{TD})} \tag{1}$$

$$V_{off} = V_{DD} \tag{2}$$

$$V_{M1} = |V_{C1} - V_{on}| \tag{3}$$

$$V_{M2} = |V_{C2} - V_{off}|, \tag{4}$$

where

$$V_{C1} = \frac{V_a}{(1 + \beta_R)^{\frac{1}{2}}} + V_{TD} \tag{5}$$

$$V_{C2} = \sqrt{\tfrac{4}{3} \cdot V_a} + V_{TD} \tag{6}$$

$$V_a = \sqrt{\frac{V_{TL}^2}{\beta_R}}, \tag{7}$$

and where

V_{TD}, V_{TL} = threshold voltages of Q_D and Q_L, respectively,
V_{DD} = supply voltage,
β_D, β_L, β_R = IGFET gain parameter of driver and load and their ratio.

The propagation delay (t_d) is directly related to the inverter-output rise time (t_r) and fall time (t_f). Since the rise-time charging current is given by $I_r = (\beta_L/2) \cdot (V_{TL})^2$, t_r may be approximated as

$$t_r = \frac{2V_{DD}C}{\beta_L V_{TL}^2}, \tag{8}$$

where C is the output capacitance and, neglecting interconnection capacitance, may be expressed in terms of β_D as

$$C = \frac{l_D^2 \beta_D}{\mu} (1 + F), \tag{9}$$

where l_D is the channel length of Q_D, μ is the mobility of carriers in the channel, and F is the numher of similar inverter gates to he driven (fan-out). If interconnection capacitance is expressed as equivalent fan-out, eq. (9) is still applicahle. Suhstituting (9) into (8) results in

$$t_r = \frac{2V_{DD}\beta_R l_D^2}{\mu \cdot V_{TL}^2} (1 + F). \tag{10}$$

Likewise, since the fall-time discharging current,

$$I_f = (\beta_D/2)(V_{DD} - V_{TD})^2 - (\beta_L/2)V_{TL}^2,$$

the fall time of the output voltage may he approximated as

$$t_f = \frac{2V_{DD}l_D^2(1 + F)}{\mu[(V_{DD} - V_{TD})^2 - V_{TL}^2/\beta_R]}. \tag{11}$$

Since t_d is proportional to $(t_r + t_f)$, we ohserve from (10) and (11) that t_d is directly proportional to l_D^2, F, and V_{DD}. A more important ohservation, perhaps, is that as V_{TL}^2/β_R increases, t_r decreases and t_f increases. Thus, depletion-load inverters designed for optimal speed have t_r and t_f nearly equal.

A final useful relationship is the power-delay product of the inverter. Using the average power for P_D for small V_{TL}^2/β_R,

$$P_D t_d \sim P_D t_r \sim (V_{DD} I_L)\left(\frac{V_{DD}C}{I_L}\right) \sim V_{DD}^2 C \sim \frac{V_{DD}^2 l_D^2 \beta_D (1 + F)}{\mu},$$

where C_D is the gate capacitance of Q_D, and $P_D t_d$ is completely independent of V_{TL}. However, for larger values of V_{TL}^2/β_R,

$$P_D t_d \sim P_D t_f \sim \frac{V_{DD}^2 \beta_D l_D^2 (1 + F)}{\mu\left[\frac{\beta_R (V_{DD} - V_{TD})^2}{V_{TL}^2} - 1\right]},$$

and $P_D t_d$ increases quadratically as $|V_{TL}|$ increases until $|V_{TL}| \sim \sqrt{\beta_R}|V_{DD} - V_{TD}|$.

As we stated earlier, the preceding approximate equations provide insight into the dependence of circuit parameters on device parameters for a depletion-load IGFET inverter. This is appropriate for characterizing the properties of any depletion-load IGFET random logic circuit, normally comprising an assortment of n-input NAND and NOR gates,

because both these logic gates can be analytically reduced to an equivalent depletion-load IGFET inverter.

2.3 Selection of V_{TL} and β_R

In this section, the method of determining the parameters of the depletion-load IGFET and the corresponding β_R are discussed. Since the equations developed in Section 2.2 are only approximate, more exact calculations were made using the circuit analysis program SERVICE.[5] In this way, the voltage dependence of V_{TL} was properly accounted for.

The objectives and constraints of the technology were chosen to he:

(*i*) Single-supply voltage $V_{DD} = -5 \pm 0.5$ volt.

(*ii*) $V_{TD} = -1 \pm 0.4$ volt at end of life.

(*iii*) $|V_{on}| \leqq |V_{TD}|$.

(*iv*) V_{M1} and $V_{M2} \geqq 0.5$ volt.

The prohlem is then, simply: Given these conditions, determine β_R and V_{TL} such that t_d is nearly a minimum for an assumed typical fan-out of five from each inverter. The net result is a family of t_d vs. V_{TL} curves. Since V_{on}, V_{M1}, and V_{M2} are functions of V_{TL}, a different β_R, the minimum value consistent with conditions (*iii*) and (*iv*) was chosen for every value of V_{TL} used. A nominal t_d vs V_{TL} curve is shown in Fig. 3, where the $P_D t_d$ product is also plotted against the same V_{TL} scale. As can be seen from the curve, the value of t_d reaches a nearly minimum constant value for $V_{TL} \sim 4.5$ volts, when $t_r \sim t_f$. We may further note that the $P_D t_d$ product increases approximately quadratically as V_{TL} increases. Based on this type of plot of all com-

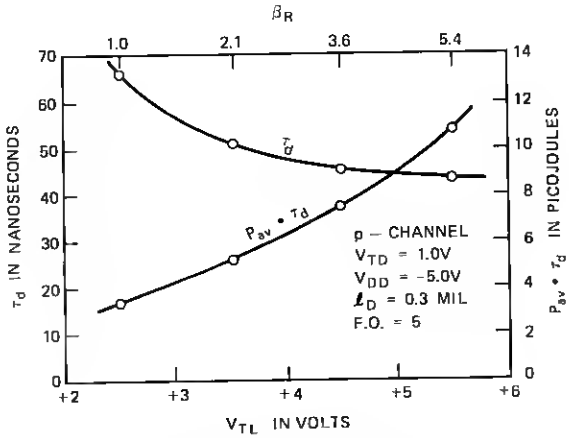

Fig. 3—τ_d and $P_{av} \cdot \tau_d$ vs. V_{TL} curve.

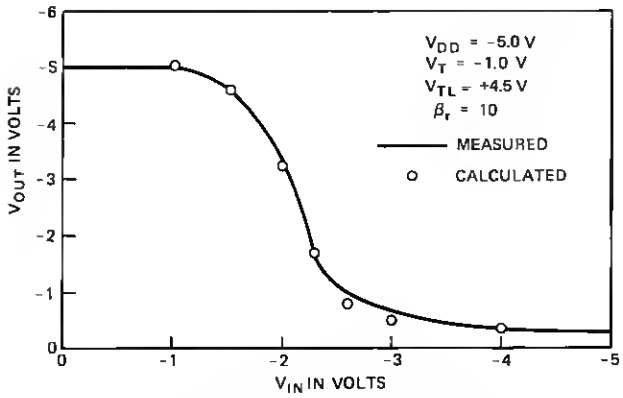

Fig. 4—Depletion-load inverter transfer curve.

binations for different limits of V_{DD} and V_{TD}, an optimal $V_{TL} = 4.5 \pm 0.5$ volt was chosen, corresponding to a minimum design β_R of 5.

Figure 4 shows a calculated and a measured dc transfer curve. The good agreement between the two is an indication of the validity of the present work.

III. DEPLETION-LOAD FABRICATION AND CHARACTERISTICS

A proven method of fabricating depletion IGFET's is the use of a selective ion implant through the gate dielectric in the IGFET channel regions. To achieve good control of the device properties, it is desirable to have the majority of the implanted ions in the silicon rather than in the gate dielectric, which requires 120 keV for the boron ions used. The resulting device no longer behaves exactly like the normal IGFET

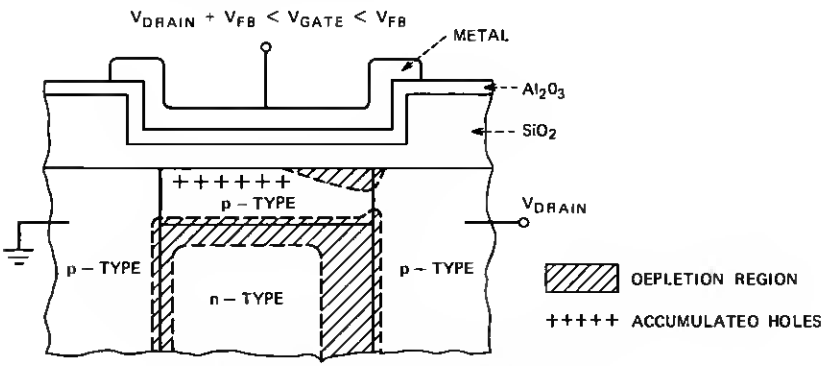

Fig. 5—Depletion IGFET cross-sectional view.

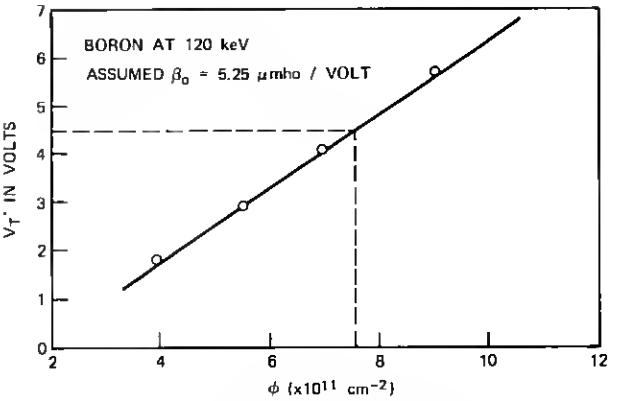

Fig. 6—Effective threshold vs. implant dose.

in which conduction takes place only in the surface inversion. It is actually a deep depletion IGFET with a subsurface channel, whose conductivity is modulated both by surface depletion and by the channel to substrate junction as shown in Fig. 5. The current-voltage characteristics of such a deep depletion IGFET have been previously described.[3]

To achieve a reproducible profile of the ion-implanted dopants in the silicon, it is desirable to minimize the duration and extent of high temperature anneal treatment after the ion implantation. Since all the diffusion processes take place before the gate oxidation, the latter is the last high temperature step. Therefore, ion implantation is performed after the gate oxidation process. The photomask step for the boron implantation utilizes a thick photoresist layer (1.4 μm) that is opaque to the 120-keV boron ions. Furthermore, since the required implantation dose of 7.6×10^{11} cm^{-2} is rather low, no damage to the gate dielectric is either expected or observed in the fabricated samples. The needed anneal[6] of implanted species is achieved in a subsequent process step when the masking SiO_2* is deposited over the whole wafer at 900°C for 20 minutes.

Figure 6 shows the effective threshold $V_T' = \sqrt{(2I/\beta)}$ as a function of the implantation dose of boron at 120 keV. The current is measured when gate and source are common and the drain biased at −5 volts. We observe that the $V_T' - Q$ curve is essentially linear over a fairly wide range of dose (2×10^{11} to 9×10^{11} cm^{-2}).

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* The metal-gate IGFET (Ref. 1) has a double layer Al_2O_3-SiO_2 for its gate dielectric. The deposited oxide is needed to serve as a mask when Al_2O_3 is selectively etched.

IV. INTERFACE CIRCUITS

To allow realization of the speed advantages offered by the depletion-load and BIGFET technologies, two buffer circuit configurations have been developed to facilitate efficient interface between inputs and outputs of BIGFET SIC's as well as to inputs and outputs of TTL(L) circuits. These two circuits are the level-shifting input circuit and the low-impedance output driver.

4.1 Input interface

It is necessary that the input voltage to an IGFET inverter be within one device threshold of substrate potential to assure complete turn-off of that inverter. Since this requirement is not met for the 1-volt threshold p-channel technology by either TTL or BIGFET output levels, the input level shifting circuit has been designed to accept these logical 1 levels. The schematic of the input circuit is shown in Fig. 7. The corresponding dc transfer curves are shown in Fig. 8. The internal feedback configuration of the level shifter produces a very sharp gain characteristic that lowers the required level for logic 1 and also provides increased noise margin and input signal wave shaping. In the design of this circuit, both the β ratio of $Q1$ to $Q2$ and the β ratio of $Q3$ to $Q4$ strongly affect the acceptable input voltage range. The β ratio of $Q1$ to $Q3$ is not critical, but may be chosen to produce minimum propagation delay of signals through the input level shifter in a specific application.

A further constraint on the β values of $Q1$ and $Q2$ is the fan-out desired from TTL(L) outputs and from BIGFET outputs into this level shifting input. During a 1 to 0 transition of the input voltage, IGFET's $Q1$ and $Q2$ conduct current from the substrate to the input node. The requirement of conducting this current to ground while maintaining a valid 0 level at the input determines the fan-out from a given output to the level shifting input circuits. Maximum 0 level V_{in} to the level

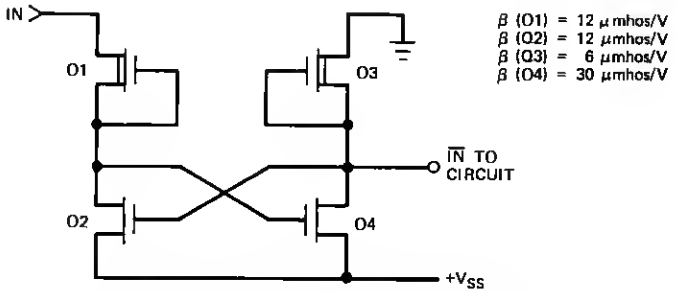

Fig. 7—Inverting level shifting input circuit.

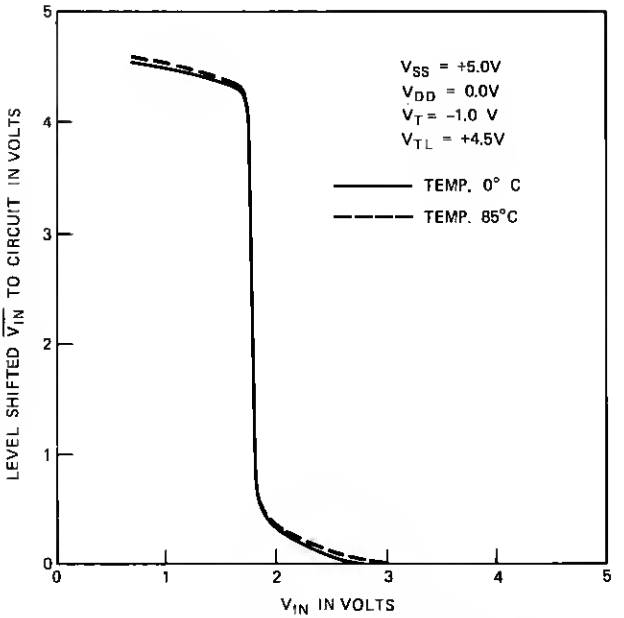

Fig. 8—Inverting level shifter transfer curves.

shifting input inverter is $V_{SS} - 3.4$ volts, which is 1.1 volts for $V_{SS} = 4.5$ volts. Allowing 0.4-volt interface noise margin requires that the input voltage be $\leqq 0.7$ volt for the 0 level. The TTL(L) output is rated at 28 mA to ground at 0.7 volt. The level shifting input inverter of Fig. 7 can conduct $\beta \times 4.2$ μA during a 1 to 0 transition, where $\beta = \beta_{Q1}$ or β_{Q2} is expressed in micromhos per volt. Therefore, the fan-out from TTL(L) to level shifting inputs is fan-out = $6667/\beta$, where $\beta = \beta_{Q1}$ or β_{Q2}. Similarly, the BIGFET output with maximum output resistance of 2.1 kilohms can conduct 0.333 mA at 0.7 volt. Therefore, fan-out from BIGFET outputs to level shifting inputs is fan-out = $79/\beta$, where $\beta = \beta_{Q1}$ or β_{Q2}.

The circuit of Fig. 7 has been used in various depletion-load circuits for both custom and general-purpose applications. It provides

	Min.	Max.
V_{in} 0	0.0	$V_{SS} - 3.4$ volts
V_{in} 1	$V_{SS} - 2.2$	V_{SS} volts.

4.2 Output Interface

The BIGFET output circuit configuration is shown in Fig. 9. This circuit provides an ideal coupling between the high-impedance IGFET's and the desired low-output impedance. The current gain provided by

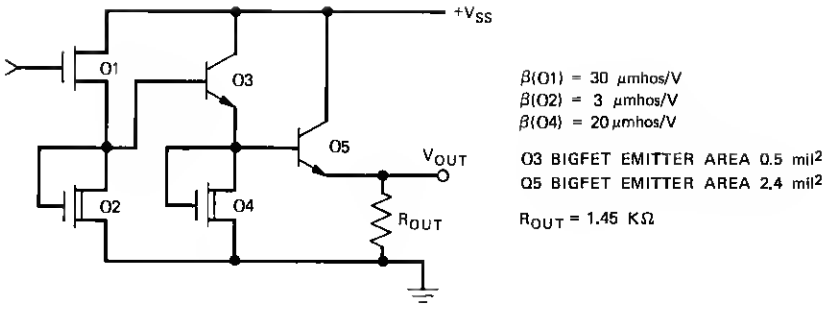

Fig. 9—BIGFET SIC output circuit.

the Darlington BIGFET structure permits the gate capacitance of $Q1$ to be as small as that normally used internally in an IGFET circut. Since average power dissipation of the output circuit is $\propto (R_{out})^{-1}$, it is desirable to make R_{out} large. But tbe maximum allowed value of R_{out} is determined by tbe input cbaracteristics of TTL(L), -240 μa at 0.4-volt input logical 0. Consequently, R_{out} is nominally 1.45 kilohms, and the other device values are as shown in Fig. 9 for this BIGFET output configuration with fan-out = 1 capability to TTL(L) circuits.

The value of R_{out}, tbe V_{be} voltage drops of $Q3$ and $Q5$ operating as a Darlington pair, and tbe BIGFET emitter area of $Q5$ are designed to prevent $Q5$ from entering tbe saturation region, which would significantly increase the turn-off time of $Q5$.

The circuit of Fig. 9 has been used in various depletion-load circuits for botb custom and general-purpose applications. It provides

	Min.	Max.
V_{out} 0	0.0	0.4 volt
V_{out} 1	$V_{SS} - 1.7$	$V_{SS} - 1.2$ volts.

V. SUMMARY

The p-channel depletion-load BIGFET process bas been demonstrated to be a successful technology for producing BIGFET SIC's. Circuit behavior bas been approximately described using simplified circuit equations, and exact circuit behavior has been cbaracterized using results from computer circuit analysis programs. Good agreement has been achieved between experimental results and circuit simulation. The application of ion implantation to the fabrication of depletion mode IGFET load devices bas been described, and a correlation is shown between the effective threshold voltage and implant dose. Finally, the input and output buffer circuits, which allow interface between BIGFET SIC's and TTL(L) circuits, are presented.

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